ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18

Stylesheet Version v18.0

Title of Invention	THE USE OF A LAYOUT-OPTIMIZATION TOOL TO INCREASE THE YIELD AND RELIABILITY OF VLSI DESIGNS

Application Number :

Confirmation Number:

First Named Applicant: Robert Allen

Attorney Docket Number: BUR920030092US1

Art Unit:

Examiner:

Search string: (4831725 or 5459690 or 5796274 or 5798937 or 6026224 or 6189132 or 6484301 or 6556658).pn

US Patent Documents

Note: Applicant is not required to submit a paper copy of cited US Patent Documents

init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
MW	1	4831725	1989-05-23	Dunham et al.			
MW	2	5459690	1995-10-17	Rieger et al.			
MW	3	5796274	1998-08-18	Willis et al.			
MW	4	5798937	1998-08-25	Bracha et al.			
MW	5	6026224	2000-02-15	Darden et al.			
MW	6	6189132	2001-02-13	Heng et al.			
MW	7	6484301	2002-11-19	Burden			
MW	8	6556658	2003-04-29	Brennan			

Signature

Examiner Name	Date
MWilczewski	3/2005

10/604987

INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

ATTY DOCKET NO.	SERIAL NO.
BUR920030092US1	Not Yet Assigned
FILING	GROUP
Concurrently Herewith	Unknown

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
MW		DE3326427	02/13/85	Germany				

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

MW			Allan et al., "Automated Redundant Via Placement for Increased Yield and Reliability", Proceedings of the SPIE - The International Society for Optical Engineering Conference, vol. 3216, 1997, pp. 114-125.
MW			Frank et al., "Yield Improvement of Wafer-Scale Integrated Systolic Structures Via Redundancy", 16th Annual IEEE Electronics and Aerospace Systems Conference and Exposition. 1983, pp. 317-322.

EXAMINER	DATE CONSIDERED
MWilczewski	3/2005

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

MW			IBM Technical Disclosure, "Yield and Reliability Enhancement Via Redundancy for VLSI Chips and Wafers," vol. 28, No. 1, 1985, pp. 36-42.
MW			Chen et al., "Layout Techniques for VLSI Yield Enhancement", Proceedings of the SPIE - The International Society for Optical Engineering Conference", vol. 4600, 2001, pp. 140-147.

EXAMINER	DATE CONSIDERED
M Wilczewski	3/2005

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